REMARKS

By the above actions, claims 28, 30, 31, 33, 34-38, 40-42, 47 and 48 have been amended, and claims 44 and 46 cancelled. Claims 28-43, 45, 47 and 48 are currently pending. In view of these actions and the following remarks, further consideration of this application is now requested.

With regard to the Examiner's objection to the specification and claims, as well as the formality rejection, under 35 U.S.C. § 112 (second paragraph), of claims 28, 33, 34, 40-42, 44 and 46, the attached substitute specification and amendments to the claims are believed sufficient to overcome each of those noted deficiencies.

Further, in order to insure consistency between the specification and the Figures, please find attached a REQUEST FOR APPROVAL OF DRAWING CORRECTIONS filed on even date herewith, which corrects Figures 3A, 5B and 6 to be consistent with the features discussed in the specification.

Turning to the prior art rejection of claims 28-48, under 35 U.S.C. 102(a), as being anticipated by the teachings of Ohtani et al (JP 2000-183356), the Applicants respectfully traverse this rejection. Specifically, the Applicants note that the Ohtani et al reference has a publication date of June 30, 2000, which is less than one year earlier than the instant filing date of April 19, 2001; therefore, since the inventors listed for Ohtani et al (JP 2000-183356) are exactly the same as the inventors of the current application, the Ohtani et al reference is not prior art to the claimed invention, see MPEP Chapter 2132.01. Therefore, it is respectfully requested that the rejection of claims 28-48 under §102(a) be withdrawn.

Finally, with regard the Examiner's provisional double-patenting rejection of claims 28, 29, 34-36, 41, 42, 45, 47 and 48, under 35 U.S.C. 101, as claiming the same invention as that of claims 1-14 of Application No. 09/837,558, this rejection is also traversed. The Applicants bring to the Examiner's attention the fact that the semiconductor devices in original claims 1-14 of Application No. 09/837,558 have been canceled and replaced by claims 31-50 which

are drawn to a method of manufacturing a semiconductor device. Therefore, since the currently claimed invention is not the same as that of Application No. 09/837,558, the instant §101 rejection above has been rendered moot and should be withdrawn.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise, which could be eliminated through discussions with applicant's representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby be expedited.

Lastly, it is noted that a separate Extension of Time Petition (one month) accompanies this response along with a check in payment of the requisite extension of time fee. However, should that petition become separated from this Amendment, then this Amendment should be construed as containing such a petition. Likewise, any overage or shortage in the required payment should be applied to Deposit Account No. 19-2380 (740756-2296).

Respectfully submitted,

Jerome W. Massie IV
Reg. No. 48,118

NIXON PEABODY LLP
8180 Greensboro Drive
McLean, Virginia 22102
(703) 770-9300
(703) 770-9400 fax

Mark-up Showing Amendments Made

IN THE ABSTRACT: (Deletions shown in strike-through since the translated abstract uses bracketing "[...]" extensively)

~~[NAME OF DOCUMENT] Document of abstract~~

~~[ABSTRACT]~~

~~[PURPOSE]~~

~~Providing a semiconductor device with a TFT structure with high reliability~~

~~[MEANS]~~

In a CMOS circuit formed on a substrate 101, a subordinate gate wiring line (a first wiring line) 102a and main gate wiring line (a second wiring line) 107a are provided in an n-channel TFT. The LDD regions 113 overlaps the first wiring line 102a and does not overlap the second wiring line 107a. Thus, when a gate voltage is applied to the first wiring line, the GOLD structure is formed, while no applying forms the LLD structure. In this way, the GOLD structure and the LLD structure can be used appropriately in accordance with the respective specifications required for the circuits.

~~[SELECTED FIGURE] Fig. 1~~

IN THE CLAIMS: (Deletions shown by conventional bracketing and additions shown as underlined)

28. (Amended) A semiconductor device including a CMOS circuit formed by an n-channel TFT and a p-channel TFT, characterized in that:

the CMOS circuit has a structure that an active layer is sandwiched by a first wiring line and a second wiring line through [an] insulating [layer] layers in only the n-channel TFT,

the active layer includes a low concentration impurity region that is in contact with [the] a channel formation region; and

the low concentration impurity region is formed to overlap the first wiring line and not to overlap the second wiring line.

30. (Amended) A semiconductor device including a CMOS circuit formed by an n-channel TFT and a p-channel TFT, characterized in that:

the CMOS circuit has a structure that an active layer is sandwiched by a first wiring line and a second wiring line through [an] insulating [layer] layers in only the n-channel TFT; and

the second wiring line has a portion of structure laminated with a first conductive layer and a second conductive layer, and a portion of structure wrapped a third conductive layer with the first conductive layer and the second conductive layer.

31. (Amended) A semiconductor device according to claim 30, characterized in that the third conductive layer has a lower resistance value than [a] the first conductive layer or the second conductive layer.

33. (Amended) A semiconductor device according to claim 30, characterized in that the third [wiring line] conductive layer is appropriately a conductive film mainly containing aluminum (Al) or copper (Cu).

34. (Amended) A semiconductor device having a pixel matrix circuit that includes a pixel TFT and a storage capacitor formed in n-channel TFT, characterized in that:

the pixel TFT has a structure that an active layer is sandwiched by a first wiring line and a second wiring line through [an] insulating [layer] layers,

the active layer includes a low concentration impurity region that is in contact with [the] a channel formation region; and

the low concentration impurity region is formed to overlap the first wiring line and not to overlap the second wiring line.

35. (Amended) A semiconductor device according to claim 34, characterized in that the first wiring line is kept at [the] a ground electric potential or at [the] a source power supply

electric potential.

36. (Amended) A semiconductor device according to claim 34, characterized in that the first wiring line is kept at [the] a floating electric potential.

37. (Amended) A semiconductor device having a pixel matrix circuit that includes a pixel TFT and a storage capacitor formed in an n-channel TFT, characterized in that:

the pixel TFT has a structure that an active layer is sandwiched by a first wiring line and a second wiring line through [an] insulating [layer] layers,

the second wiring line has a portion of structure laminated with a first conductive layer and a second conductive layer, and a portion of structure wrapped a third conductive layer with the first conductive layer and the second conductive layer.

38. (Amended) A semiconductor device according to claim 37, characterized in that the third conductive layer has a lower resistance value than [a] the first conductive layer or the second conductive layer.

40. (Amended) A semiconductor device according to claim 37, characterized in that the third [wiring line] conductive layer is appropriately a conductive film mainly containing aluminum (Al) or copper (Cu).

41. (Amended) A semiconductor device having a pixel matrix circuit and a driver circuit that are formed on [the] a same substrate, characterized in that:

a pixel TFT included in the pixel matrix circuit and an n-channel TFT included in the driver circuit have a structure that an active layer is sandwiched by a first wiring line and a second wiring line through [an] insulating [layer] layers; and

the first wiring line connected to the pixel TFT is kept at [the] a fixed electric potential or [the] a floating electric potential, and the first wiring line connected to the n-channel TFT included in the driver circuit is kept at [the] a same level of electric potential as the second wiring line connected to the n-channel TFT included in the [said] driver circuit.

42. (Amended) A semiconductor device according to claim 41, characterized in that the active layer includes a low concentration impurity region that is in contact with [the] a channel formation region; and

the low concentration impurity region is formed to overlap the first wiring line and not to overlap the second wiring line.

47. (Amended) A semiconductor device[, characterized in that the semiconductor device] according to any one of claims 28 to 46, the semiconductor device is an active matrix liquid crystal display or an active matrix EL display.

48. (Amended) A semiconductor device[, characterized in that the semiconductor device] according to any one of claims 28 to 46, the semiconductor device is selected from a video camera, a digital camera, a projector, a projection TV, a goggle type display, an automobile navigation system, a personal computer, or a portable information terminal.